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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,576	12/29/2000	Manoj Khare	42390P9874	1630

7590 12/18/2003

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EXAMINER
HO, THANG H

ART UNIT	PAPER NUMBER
2188	11

DATE MAILED: 12/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,576	KHARE ET AL.	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-18,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated 10/15/2003. The applicant's remarks and amendment were considered with the results that follow.

2. Claims 1-21 are pending in this application for examination. Claims 1, 3-4, 6, 8, 13-15, 18 and 20 have been amended, claims 5 and 19 have been cancelled and no new claim has been added. Therefore, claims 1-4, 6-18, and 20-21 remain pending in the application.

3. The missing Oath/Declaration for inventor Kenneth C. Creta is withdrawn due to Amendment filed on 10/15/2003.

4. The objection to the drawings is withdrawn due to the Amendment filed on 10/15/2003.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamaguchi et al. (USPN: 5,737,568); hereinafter Hamaguchi;

Referring to claim 1, Hamaguchi discloses an invention to control cache coherency in multiprocessor system (figure 2) utilizing a shared memory (26) including receiving a request to read a modified cache line at the responding node (21) of a shared

memory multiprocessor architecture from a requesting node (22) of the shared memory multiprocessor architecture; responding to the request by updating a memory at a home node with data read from the modified cache line and provide an answer to the requesting node, wherein the home node is different from the corresponding node (e.g. see figure 2, column 4, lines 12 et seq. and column 5, lines 1-18);

Referring to claim 2, Hamaguchi further discloses the answer containing a copy of the data read from the modified cache line (e.g. see column 5, lines 8 et seq.);

Referring to claim 3-4 and 7, and, Hamaguchi discloses the response containing the status of the modified cache line utilizing MESI protocol. Figure 7 shows the transition of the modified cache from a modified state (1) to an invalid state (2) and a modified cache from modified state (1) to a shared state (4);

Referring to claim 6, Hamaguchi discloses the updating of the memory at the home node and providing a completion response to the requesting node (e.g. see column 5, lines 7 et seq.);

Referring to claim 8, Hamaguchi discloses a shared memory multiprocessor system (figure 2) comprising a plurality of node controllers (21-24) and a switch (25) coupled to each of the plurality of node controllers configured to: transmit a read request regarding a modified cache line from a first node controller (21) of the plurality of node controllers through the switch to a second node controller (22) of the plurality node controllers, wherein the second node controller is distinct from the first node controller; and in response to receiving the read request regarding the modified cache line, the second node controller instructs the switch to update a home memory (23) residing

exclusively on a third node controller of the plurality of node controllers (e.g. see columns 9 and 10);

Referring to claim 12, Hamaguchi discloses an implicit write-back, initiated by a responding node, in response to a read request directed to a modified cache line at the responding node (e.g. see column 6, lines 14-20);

Referring to claim 13, the implicit write-back including information causing the read request to be answered and a home memory to be updated (e.g. see figure 2, column 5, lines 4-18);

Referring to claim 14, the further limitation of the implicit write-back further includes information identifying the state information of the modified cache line is taught by Hamaguchi (e.g. see figure 3).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamaguchi in view of Flynn et al. (USPN: 5,222,224), hereinafter Flynn.

The teachings of Hamaguchi have been discussed supra. Hamaguchi does not teach the usage of a switch or system control unit (SCU) for maintaining a presence vector containing the status of a cache line for each participating node controller of the

plurality of node controllers, and whether the corresponding participating node controller contains a copy of the contents stored in the home memory. Flynn teaches the usage of a centralize SCU to maintain a copy of cache directory as well as the presence vector of each processor caches (e.g. column 5, lines 14 et seq.). It would have been prima facie obvious to one skilled in the art at the time of the invention was made to implement a shared memory multiprocessor system as being taught by Hamaguchi and modify the invention to include a switch as taught by Flynn to improve data consistency between cache memories and the main memory, to speedup lookup time and to reduce bus requirements of each processor in a multiprocessor system.

9. Claims 15-18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamaguchi (USPN: 5,737,568).

The teachings of Hamaguchi have been discussed supra with respect to claims 1-7. Hamaguchi does not teach the usage of a computer readable medium of instructions to be implemented on a client computer as being claimed in claims 15-21. However, one of ordinary skill in the art would have recognized that computer readable medium (i.e., floppy, cd-rom, etc.) carrying computer-executable instructions for implementing a method, because it would facilitate the transporting and installing of the method on other systems, is notoriously well-known in the art. For example, a copy of the Microsoft Windows operating system can be found on a cd-rom from which Windows can be installed onto other systems, which is a lot easier that running a long cable or hand typing the software onto another system. Therefore, it would have been prima facie obvious to

put Hamaguchi's program on a computer readable medium, because it would facilitate the transporting, installing and implementing of Hamaguchi's program on other systems.

Response to Arguments

10. Applicant's arguments filed 10/15/2003 with respect to Claims 1-4, 6-18 and 20-21 have been fully considered but they are not persuasive.

Applicants asserted:

(a) Hamaguchi does not disclose receiving a request to read a modified cache line; receiving such request at a responding node from a requesting node; and responding to the request to read a modified cache line by updating a memory at a home node with data read from the modified cache line, and by providing an answer to the requesting node.

(b) Neither Hamaguchi, nor Flynn, nor their combination disclose, teach, or suggest the respective combination of elements of claims 9-11.

Examiner respectfully traverses Applicant's remarks for the following reasons:

With respect to (a), Hamaguchi clearly discloses in FIG. 3 and column 4 line 66 through column 5, line 18 that the requesting node (processor 22) tries to perform a **read** operation in order to gain access to the data of address 1000 and the processor 22 recognizes that the data are stale (modified) since entry is in the SHS state. Hence, the processor 22 generates a transaction on the bus 25 as a cache miss. The cache memory control device of the responding node (processor 21) monitors the transaction and

responds to the read request by placing the valid data on the bus 25 thereby, updating the main memory storage 26 and providing an answer to processor 22 (the requesting node).

With respect to (b), before addressing the argument, Examiner would like to emphasize that in considering a 35 USC 103 rejection, it is not strictly necessary that a reference or references explicitly suggest the claimed invention (this is tantamount to a 35 USC 102 reference if the modifications would have been obvious to those of ordinary skill in the art). It has been held that the test of obviousness is not whether the features of a secondary reference may be bodily incorporated into the primary references' structure, nor whether the claimed invention is expressly suggested in any one or all of the references; rather, the test is what the combined teachings of the reference would have suggested to those of ordinary skill in the art. See In re Keller et al., 208 U.S.P.Q 871.

In addition, in response to Applicant's argument that the Examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Hamaguchi teaches the invention substantially as claimed including a plurality of system control unit (SCU) for maintaining a presence vector containing the status of a cache line for each participating node controller of the plurality of node controllers, and whether the corresponding participating node controller contains a copy of the contents

stored in the home memory (column 4, lines 51-65). However, Hamaguchi fail to teach a centralized/integrated SCU. Flyn, on the other hand, teaches the method of insuring cache consistency for use in a multi-processing system utilizing an integrated system control unit (SCU) wherein the means for maintaining a copy of a cache directory as well as the presence vector of each processor cache are disposed on an integrated SCU (see column 5, lines 14-35). One having ordinary skill in the art would recognize that by incorporating Flyn's method of integrated system control into Hamaguchi's system and method would provide improvement in data consistency between cache memories and the main memory, faster lookup time, and reducing bus requirements of each processor in a multi-processing system. Moreover, according to In re Larson 144 USPQ 347, CCPA 1965, to make integral is not generally given patentable weight; in fact this decision was later upheld for the integration of electrical components onto a single medium according to In re Tomoyuki Kohno 157 USPQ 275 1968; thus, for the purposes of rejection, integration of SCU is not seen to alter the scope of the present invention.

Therefore, the rejection of claims 1-4, 6-18 and 20-21 is deemed to be proper. Hamaguchi's and Flyn's teachings, taken alone or in concert, disclose each and every element recited within claims 1-4, 6-18 and 20-21.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Thang Ho
Art Unit 2188
December 12, 2003

Kevin L. Ellis
Primary Examiner

Kevin L. Ellis